A Timing Jitter Insensitive Logic Gate Using Tunable Gain Dynamics in an SOA and Optical Thresholding

Yue Tian¹, Mable P. Fok², Paul R. Prucnal¹
¹Lightwave Communication Research Laboratory, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA
²Lightwave and Microwave Photonics Laboratory, College of Engineering University of Georgia, Athens, GA 30606, USA
E-mail: yuetian@princeton.edu

Abstract: We experimentally demonstrate a reconfigurable and timing-jitter insensitive AND/NOT gate based on tunable gain dynamics in a semiconductor optical amplifier and optical thresholding. The measured jitter tolerance is up to ±50 ps or ±25 ps for the AND/NOT gate.

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1. Introduction

All-optical logic gates have received considerable attention in the field of next-generation optical networks and optical computing systems for optical signal processing functions [1-4]. Several approaches have been demonstrated to realize various logic functions using highly nonlinear fibers [1] or semiconductor optical amplifiers (SOA) [2-4]. However, all of them are sensitive to the timing jitter of the input signals.

In this paper, we propose and demonstrate a reconfigurable AND/NOT logic device based on the gain dynamics of an SOA and optical thresholding of a nonlinear optical fiber loop mirror (NOLM) [5]. Reconfiguration of the logic function can be easily achieved by changing the driving current of the SOA. Combined with the adjustable threshold level of the optical thresholder, the time window of the jitter tolerance can be tuned as well. The experimental results show that the timing jitter tolerance of AND gate is up to ±50 ps and ±25 ps for NOT operation, which is the highest to our best knowledge. With high timing-jitter tolerance, the proposed all-optical logic gate can be used for various applications in all-optical systems and networks, such as signal regeneration, optical switching and synchronization.

2. Principles and Experimental Setup

The gain dynamics of a short SOA, with pump light injection, is governed by the rate equation as follows [6]:

\[
\frac{dN'(t)}{dt} = \frac{N'(t)}{r} - \frac{N'(t)}{\tau} - \frac{\Gamma_p}{E_p} N'(t) I(t)
\]

where \(N'(t)\) is the carrier density above transparency, \(N'_{rest}\) is the resting carrier density in the absence of pump light, \(r\) is the carrier lifetime, \(I(t)\), \(\Gamma_p\), \(a_p\) and \(E_p\) represent the input light intensity, the mode confinement factor, the differential gain coefficient, and the photon energy, respectively. The sign of \(\Gamma_p\) could be either positive (gain depletion) or negative (gain pumping). Fig.1 shows the setup of the proposed reconfigurable timing-jitter insensitive logic gate. It has two input ports for pulse inputs and has the driving current and threshold level as its tunable parameters. The 1480-nm input pulses are received at input port 1 and directed into the SOA (Kamelian NL-L1-C-FA-1550). At this wavelength the optical pulses can either create gain pumping or gain depletion effect in the SOA, depending on the driving condition [6]. The 1550-nm pulses launched into input port 2 travel through the SOA in the opposite direction, and experience the gain change. Then the following thresholder based on a Ge-doped NOLM [5] eliminates the pulses lower than the threshold level and unifies the pulse power with higher power level.

Fig. 1. (a) Experimental setup of reconfigurable and timing jitter insensitive logic gate. Experimental results of AND gate: Input 1 at 1479 nm (b), Input 2 at 1549 nm (c), Output (d) and Output when input 2 lags input 1 by 50 ps (e) and 100 ps (f). Experimental results of NOT gate: Input 1 at 1479 nm (g), Probe at 1549 nm (h), Output (i) and Output when Probe lags input 1 by 25 ps (j) and 50 ps (k). CW: continuous wave; PC: polarization controller; MZM: Mach-Zehnder modulator; SOA: semiconductor optical amplifier.
When the SOA is driven by low current, specifically 15 mA in our experiment, the 1480-nm light generates the gain pumping effect ($\Gamma_p < 0$). Thus every 1480-nm pulse from Input 1 increases the carrier density, according to Equation (1), and consequently boosts the gain of the SOA. The counter-propagating 1550-nm pulses experience the gain change, resulting in an amplitude change. With proper threshold level, the thresholder can let though the 1550-nm pulses boosted by 1480-nm pulses but block the ones without boosting. Therefore, only if input 1 and 2 are both present, the output comes out from the logic gate, which corresponds to an AND operation of input 1 and 2.

With high driving current injected into the SOA, 75 mA here, the 1480-nm light changes its role to create gain depletion ($\Gamma_p > 0$). Then the 1550-nm pulses from input port 2 experience very little gain when the gain is depleted by 1480-nm light. Otherwise, the 1550-nm pulses are amplified with a higher gain. The thresholder is set to the proper level to distinguish the output in these two cases. Thus, if we keep pulse train at input 2 always available as a probe signal, the output is a NOT operation on input 1. As a result, the proposed logic gate can be reconfigured by simply changing the SOA’s driving current and adjusting the threshold level if necessary.

Another feature of the proposed logic gate is its high timing-jitter tolerance. From equation (1), after the optical pump disappears, the carrier density exponentially decays back to the rest level with time constant of $\tau$. Therefore after each stimulation (gain pumping or depletion) by the 1480-nm pulse, there is a small time window before the carrier density recovers to the original rest state. Within this time window, the 1550-nm pulses can still be affected by gain pumping/depletion. Although the effect becomes weaker gradually as time, resulting in the output amplitude change, the following thresholder can correct the unequal amplitude and keep the same output level for all input within the time window. Moreover, by tuning the driving current to the SOA, the rest level of the carrier density can be changed, which consequently changes the time-window length. In this way, we can reconfigure not only the logic function but also the timing-jitter tolerance window by adjusting the driving current and threshold level.

3. Experimental Results

In the experiment, a mode-locked fiber laser at 1549 nm is used to generate a 10-GHz pulse train. A 1479-nm continuous wave (CW) signal is carved into a 10-GHz pulse train by a Mach-Zehnder modulator (MZM). Then the two pulse trains are modulated by different data patterns to obtain different bit combinations for logical operations. Fig. 1(b) and (c) show the input 1479-nm and 1549-nm pulses, with 300-ps spacing between adjacent bits. Their pulse widths are ~30 ps and ~9 ps respectively. A 1480-nm band SOA is used to compensate the power loss due to amplitude modulations. The output from the logic gate is shown in Fig. 1(d). When the driving current is set at 15 mA, the output pulse shows up only when both inputs are present, which is consistent with AND logic. To verify the timing-jitter insensitivity, we also investigate the situation when the two inputs are not aligned in time. The 1549-nm pulses (input 2) are shifted continuously to a later time position, with all other parameters unchanged. With 50-ps lag, as illustrated by Fig. 1(e), the output keeps the same output level with no-lag output in Fig. 1(d). The timing lag is increased up to 100 ps, until the output pulse level starts to decrease and becomes noisy, which means the output level from the SOA reaches the threshold level. Thus, the AND gate allows ±50-ps timing jitter between the two inputs.

For the NOT gate, the driving current of the SOA is changed to 75 mA, to enable the gain depletion effect by the 1479-nm input. The threshold level is also adjusted accordingly to distinguish the output with and without the gain depleted. Input 2 at 1549 nm acts as a probe light. As illustrated in Fig. 1(i), when a pulse enters Input 1, the SOA cannot provide enough gain to boost the Probe pulse above the threshold level, so the output shows no pulse. Therefore the function of a NOT gate is demonstrated. To test the timing-jitter tolerance of the NOT gate, the probe pulse is shifted to lag Input 1 pulse by up to 50 ps, when the output level reaches the threshold level. Fig. 1(j) and(k) show the output results of 25-ps and 50-ps lags respectively. No obvious change is observed comparing with the output without timing shift in Fig. 1(i). Therefore the NOT gate allows ±25-ps timing jitter between the input and probe. The different timing-jitter tolerances are because of different driving currents applied onto the SOA.

4. Conclusion

We present a reconfigurable optical logic gate based on an SOA and an optical thresholder with high timing-jitter tolerance. The proposed logic gate employs the tunable gain dynamics of the SOA with 1480-nm input pump to achieve AND or NOT logical function. The slow recovery process of gain pumping/depletion is utilized to make the logic operation insensitive to timing jitter. By changing the threshold level, the timing-jitter tolerance window is also tunable. Measured timing jitter tolerance is up to ±50 ps for AND operation and ±25 ps for NOT operation.

References